present invention are not intended to be interpreted as excluding the existence of additional embodiments that also incorporate the recited features.

[0013] In one embodiment and referring to Figure 1, a chopper-stabilized NMOS depletion mode operational amplifier circuit 10 is provided. A clock generator 12 develops clock signals 14, 16 that interface to chopping switches 18, 20 surrounding a first amplification stage 22. The chopping function provided by chopping switches 18, 20 modulates the offset of first amplification stage 22 to the clock frequency, which is outside a signal bandwidth of interest and thus easily filtered out. In one embodiment, at least one additional amplifier stage is present. In the illustrated embodiment, two additional amplifier stages 24 and 26 are present. Offsets in such additional amplifier stages 24, 26 are attenuated by at least the gain of first amplification stage 22. Each of the circuits shown is implemented utilizing NMOS depletion mode technology.

[0014] An interface between clock generator 12 and chopping switches 18 and 20 is provided by one or more buffered field effect transistor logic (BFL) level shifting/inverter circuits 28, 30. Two BFL level shifting circuits 28, 30 are provided for operational amplifier 10 to accommodate differential inputs INN and INP, which are controlled by different timing phases represented by clock signals 14, 16. (As used herein, either differential input signal INN or INP is considered an "input signal.") Due to the negative threshold voltages of field effect transistors (FETs) in NMOS depletion mode circuits, first BFL level shifting/inverter circuit 28 provides a first chopping signal 32 and a level shifted first chopping signal 34. Level shifted first chopping signal 34 is a replica of first chopping signal 32, but level shifted to voltages required for chopping switch 20. Similarly, second BFL level shifting/inverter circuit 30 provides a second chopping signal 36 and a level shifted second chopping signal 38. In the embodiment represented in Figure 1, NMOS depletion mode chopping switch 18 is responsive to both first chopping signal 32 and second chopping signal 36 to chop a differential input signal (INN and/or INP) to first amplification stage 22. The chopped input signal thereby produced is shown as a differential signal, CINA and CINB. Similarly, NMOS depletion mode chopping switch 20 is responsive to level shifted first chopping signal 34 and level shifted second chopping signal 38 to chop the amplified chopped output signal of first amplification stage 22. The amplified chopped output signal is shown as another *differential* signal, 40 and 42. The result of the chopping performed by chopping switch 20 is that a chopper-

stabilized output signal is produced. The chopper-stabilized output signal is shown as a differential signal, CSOUTA and CSOUTB. In one embodiment, this differential signal is itself provided as an output. However, in the embodiment of amplifier 10 represented in Figure 1, further amplification of this signal takes place, and it is converted into a single-ended output OUT. Output OUT is a chopper-stabilized output signal produced in amplifier 10 as a result of the chopping process.

[0015] One embodiment of an NMOS depletion mode circuit 44 suitable for use as BFL level shifting/inverter circuit 28 or 30 is shown schematically in Figure 2. Circuit 44 comprises an NMOS depletion mode inverter circuit 46 having an input 48 for a clock signal (14 or 16 in Figure 1). Inverter circuit 46, which is part of circuit 44, comprises field effect transistors (FETs) Q1 and Q2 and is responsive to an input signal at 48 to generate an inverted output 50. Inverted output 50 is applied to a buffered field effect transistor logic (BFL) stage 52. BFL stage 52 comprises FET Q3, which has a gate and a channel, and FET Q4, which also has a gate and a channel. In addition, a voltage drop circuit 54 is connected in series with the channels of FETs Q3 and Q4. In the circuit shown in Figure 2, voltage drop circuit 54 includes one or more diode-connected FETs, for example, FETs Q5 and Q6. Output 60 is taken from node 56, between the channel of FET Q3 and voltage drop circuit 54, and output 62 is taken from node 58, between voltage drop circuit 54 and the channel of Q4.

[0016] Referring to Figures 1 and 2, BFL level shifting/inverter circuit 28, when implemented as circuit 44 shown in Figure 2, connects clock signal 14 to input 48. Chopping signal 32 is produced at output 62, and level shifted chopping signal 34 is produced at output 60. Another circuit having the same topology as circuit 44 is also used as BFL level shifting/inverter circuit 30, with clock signal 16 connected to input 48. In this case, chopping signal 36 is produced at output 62, while level shifted chopping signal 38 is produced at output 60.

[0017]

Another embodiment of an NMOS depletion mode inverter circuit 64 is represented by the schematic diagram shown in Figure 3. Circuit 64 can be used as an alternative for circuit 44 of Figure 2 in amplifier circuit 10 of Figure 1 or in other circuits. Circuit 64 differs from circuit 44 in that the voltage drop circuit in circuit 64 is a *resistor R1*, which can readily be produced using the NMOS depletion mode process. This embodiment

facilitates high reliability because a negative direct current (DC) bias is kept on all FETs (i.e., Q1, Q2, Q3, and Q4 of circuit 64) with respect to their respective sources. Either circuit 64 or circuit 44 are suitable for fabrication using SiC technology. Input 48 and outputs 60 and 62 of circuit 64 are used in the same manner as the corresponding inputs and outputs of circuit 44.

[0018] Referring to Figure 4, the remaining circuitry of chopper stabilized NMOS depletion mode operational amplifier 10 are conventional. In the topology shown in Figure 4, chopping switch 18 has threshold voltages that are negative with respect to the drains and sources of (and thus, the channels of) FETs Q7, Q8, Q9, and Q10. Similarly, chopping switch 20 has threshold voltages that are negative with respect to the drains and sources of FETs Q11, Q12, Q13, and Q14. Differences in source potentials for switches 18 and 20 require level shifting of drive voltages applied to the gates of their respective FETs to turn the switches on and off. This level shifting is provided by BFL level shifting circuits 28 and 30 (not shown in Figure 4). The use of either circuit 44 or 64 as a BFL level shifting circuit allows an inverter to drive both sets of chopping switches simultaneously without the use of additional level shifting circuitry. Offsets in amplifier 10 are removed dynamically so that offset drift and flicker noise are substantially reduced or minimized.

[0019] In one embodiment, amplifier circuit 10 is implemented in NMOS depletion mode silicon carbide (SiC) technology (i.e., fabricated on a silicon carbide substrate), and thus is a chopper-stabilized, silicon carbide NMOS depletion mode operational amplifier. In this embodiment, circuit 10 is capable of operation at much higher temperatures than is possible with conventional silicon or silicon on insulator (SOI) technologies. For example, SiC circuits are capable of operation at temperatures above 300 degrees Celsius. Thus, embodiments of amplifier 10 fabricated using SiC technology can be operated at temperatures over 300 degrees Celsius without cooling, and located at or near sensors in high-temperature environments. Noise pickup will also be reduced because, in such cases, circuit 10 can be located at a point much closer to the sensor than if cooling were required.

[0020]

Although NMOS depletion mode SiC technology is especially suitable for use in conjunction with or in embodiments of the present invention, in other embodiments, other NMOS depletion mode technologies are used. However, the temperature limitations